WHAT IS CLAIMED IS:

1. A method for testing semiconductor components comprising:

providing a substrate containing the components;

providing an interconnect comprising a plurality of interconnect contacts configured to electrically engage the components;

providing a switching network in electrical communication with the interconnect contacts configured to control the interconnect contacts to selectively apply test signals to selected components, to electrically isolate defective components and to transmit read test signals from selected groups of components;

applying test signals through the switching network and the interconnect contacts to the components; and

controlling the test signals using the switching network to perform a selected test on the components.

2. The method of claim 1 wherein the interconnect electrically engages all of the components on the substrate at a same time.

3. The method of claim 1 wherein the selected test comprises functionality testing.

4. The method of claim 1 wherein the selected test comprises parametric testing.

5. The method of claim 1 wherein the selected test comprises burn-in testing.

6. The method of claim 1 wherein the substrate comprises a wafer, a panel, a leadframe or a module.

7. The method of claim 1 wherein the components comprise dice, packages or BGA devices.

8. A method for testing semiconductor components comprising:

providing a substrate containing the components and a plurality of component contacts on the components;

providing an interconnect comprising a plurality of interconnect contacts and a switching network in electrical communication with the interconnect contacts;

placing the component contacts and the interconnect contacts in physical and electrical contact;

transmitting test signals for performing functionality tests through the interconnect contacts to the components using the switching network to multiply and selectively transmit the test signals;

electrically isolating at least one non-functional component using the switching network;

transmitting write test signals for performing parametic testing through the interconnect contacts to selected components using the switching network to multiply and selectively transmit the write test signals; and

transmitting read test signals from selected groups of components using the switching network to group the components.

9. The method of claim 8 further comprising transmitting burn-in test signals to the components using the switching network to electrically isolate at least one defective components.

10. The method of claim 8 wherein the interconnect contacts electrically engage all of the component contacts on the substrate at a same time.

11. The method of claim 8 wherein the placing step is performed using a wafer prober.

12. The method of claim 8 wherein the placing step is performed using a carrier.

13. The method of claim 8 wherein the substrate comprises a wafer and the placing step is performed using a wafer prober.

14. The method of claim 8 wherein the substrate comprises a panel or a leadframe and the placing step is performed using a carrier.

15. A method for testing semiconductor components comprising:

providing a substrate containing the components;

providing a carrier configured to hold the substrate;

providing an interconnect on the carrier comprising a plurality of interconnect contacts configured to electrically engage the components;

providing a switching network on the interconnect configured to control the interconnect contacts to selectively apply test signals to the components;

applying test signals through the switching network and the interconnect contacts to the components; and

controlling the test signals using the switching network to perform a selected test on the components.

16. The method of claim 15 wherein the carrier comprises a base, a cover and a force applying mechanism.

17. The method of claim 15 wherein the carrier comprises an alignment member configured to align the substrate on the interconnect.

18. The method of claim 15 wherein the switching network is contained on a die attached to the interconnect.

19. The method of claim 15 wherein the interconnect comprises a semiconductor material and the switching network compress a plurality active electrical switching devices in the semiconductor material.

20. The method of claim 15 wherein the substrate comprises a panel and the components comprise semiconductor packages.

21. The method of claim 15 wherein the substrate comprises a leadframe and the components comprise semiconductor packages.

22. A method for testing semiconductor components comprising:

providing a substrate containing the components;

providing a carrier configured to hold the substrate;

providing a switching network on the carrier configured to control test signals to the components;

placing the substrate in the carrier;

performing a functionality test by applying functionality test signals through the switching network to the components; and

performing a burn-in test by applying burn-in test signals through the switching network to the components.

23. The method of claim 21 further comprising performing a parametric test by applying parametric test signals through the switching network to the components.

24. The method of claim 21 wherein the substrate comprises a wafer, a panel, a leadframe or a module substrate.

25. The method of claim 21 wherein the carrier comprises a base, a cover and a force applying mechanism.

26. The method of claim 21 wherein the carrier comprises an alignment member configured to align the substrate on the interconnect.

27. The method of claim 21 wherein the carrier comprises an interconnect and the switching network is on the interconnect.

28. A system for testing semiconductor components comprising:

a substrate containing the components;

an interconnect comprising a plurality of interconnect contacts configured to electrically engage all of the components on the substrate at a same time; and

a switching network in electrical communication with the interconnect contacts configured to selectively apply test signals to selected components, to electrically isolate defective components and to transmit read test signals from selected groups of components.

29. The system of claim 28 further comprising a carrier configured to hold the substrate and the interconnect.

30. The system of claim 28 wherein the substrate comprises a wafer, a panel, a leadframe or a module.

31. The system of claim 28 further comprising a tester in electrical communication with the interconnect contacts having tester resources expanded by the switching network.

32. The system of claim 28 further comprising a base for mounting the interconnect, a cover for holding the

substrate, and a force applying mechanism for biasing the substrate and the interconnect together.

33. The system of claim 28 further comprising an alignment member configured to align the substrate on the interconnect.

34. A system for testing semiconductor components comprising:

a substrate containing the components;

a carrier configured to hold the substrate;

an interconnect on the carrier comprising a plurality of interconnect contacts configured to electrically engage the components; and

a switching network on the interconnect configured to control the interconnect contacts to selectively apply test signals to the components, to electrically isolate defective components and to transmit and to receive read test signals from selected groups of components.

35. The system of claim 34 wherein the carrier comprises a base wherein the interconnect is mounted and a force applying mechanism for biasing the substrate and the interconnect together.

36. The system of claim 34 wherein the carrier comprises an alignment member for aligning the substrate to the interconnect.

37. The system of claim 34 wherein the substrate comprises a wafer, a panel, a leadframe or a module.

38. The system of claim 34 wherein the interconnect is configured to electrically engage all of the components on the substrate at a same time.

39. The system of claim 34 wherein the substrate comprises a wafer and the components comprise semiconductor dice.

40. The system of claim 34 wherein the substrate comprises a panel and the components comprise semiconductor packages.

41. The system of claim 34 wherein the substrate comprises a leadframe and the components comprise semiconductor packages.

42. A system for testing semiconductor components comprising:

a substrate containing the components;

a testing apparatus configured to handle the substrate;

an interconnect on the testing apparatus comprising a plurality of interconnect contacts configured to electrically engage all of the components on the substrate at a same time;

a tester in electrical communication with the interconnect contacts configured to generate and analyze test signals and having tester resources determined by a signal generating and analyzing capability thereof; and

a switching network on the interconnect in electrical communication with the interconnect contacts configured to selectively apply the test signals to selected components, to electrically isolate defective components and to expand the tester resources by reading the test signals from selected groups of components.

43. The system of claim 42 wherein the testing apparatus comprises a wafer prober.

44. The system of claim 42 wherein the testing apparatus comprises a carrier configured to hold the substrate for burn-in testing.

45. The system of claim 42 wherein the testing apparatus comprises a base for holding the substrate and a force applying mechanism for biasing the substrate and the interconnect together.

46. The system of claim 42 wherein the testing apparatus comprises an alignment member configured to align the substrate to the interconnect.

47. The system of claim 42 wherein the interconnect comprises a plurality of interconnect contacts comprising conductive pockets or conductive projections.

48. A system for testing semiconductor components comprising:

a substrate containing the components;

a carrier configured to hold the substrate and to apply test signals to the components on the substrate, the carrier comprising an interconnect including a plurality of interconnect contacts configured to electrically engage the components, a force applying mechanism configured to bias the substrate and the interconnect together, and an alignment member configured to align the substrate on the interconnect; and

a switching network on the interconnect in electrical communication with the interconnect contacts configured to control the interconnect contacts and test signals to the components.

49. The system of claim 48 wherein the switching network comprises a die on the interconnect.

50. The system of claim 48 wherein the carrier comprises an electrical connector and the system further

comprising a tester in electrical communication with the electrical connector.

51. The system of claim 48 wherein the system further comprises a tester and the switching network is configured to expand resources of the tester by transmitting read test signals from selected groups of components.

52. The system of claim 48 wherein the switching network comprises a plurality of active electrical switching devices.

53. The system of claim 48 wherein the substrate comprises a wafer and the components comprise dice on the wafer.

54. The system of claim 48 wherein the substrate compress a leadframe and the components comprise packages on the leadframe.

55. The system of claim 48 wherein the substrate comprises a panel and the components comprise packages on the panel.